REMARKS

Claims 1-21 are pending in this application. By this Amendment, Applicant amends claims 1, 2, 8, 14 and 16.

Claims 2 and 16 was rejected under 35 U.S.C. § 112, second paragraph, for allegedly being indefinite. Applicant has amended claims 2 and 16 to correct the informality noted by the Examiner. It is noted that the feature of "said one of the at least two conductor layers that is omitted is disposed within said multi-layer substrate" is shown in Fig. 2 of the originally filed application which clearly shows the omitted portion 32 of the conductor layer 24 being within the multilayer substrate 12. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Claims 1-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mandai et al. (U.S. 5,227,739). This rejection is respectfully traversed.

Claim 1 has been amended to recite:

> "A resonator comprising:
> a multi-layer substrate having an upper and lower surface, and including at least two conductor layers which include at least two grounding conductor layers and a plurality of dielectric layers, one of the at least two grounding conductor layers being disposed on the lower surface of the multi-layer substrate;
> a strip line disposed between the at least two grounding conductor layers;
> a microstrip line disposed on the upper surface of said multi-layer substrate; and
> a through hole formed in said dielectric layers to connect said strip line to said microstrip line;
> wherein at least a portion of the one of the at least two conductor layers that is closest to said microstrip line and faces the microstrip line is omitted;
> **said microstrip line defines a microstrip line resonator;**
> **at least one of said plurality of dielectric layers, at least one of said at least two grounding conductor layers and said strip line d fin a strip line resonator; and**
> **a ingle resonator is d fin d by said microstrip line resonator and said trip line resonator.**" (Emphasis Added)

Claims 8 and 14 have been amended to recite features that are similar to the features recited in claim 1, including the emphasized features.

The Examiner alleged that Mandai et al. teaches all of the features recited in claims 1, 8 and 14 of the present application, including a microstrip line 9 which is connected to the strip line via a through hole V1. However, element 9 of Mandai et al. is disclosed as being a "conductive land" which is provided to connect the conductive film 4 to a terminal X2. The conductive land 9 of Mandai et al. is also provided to mount an electronic component thereon.

In contrast to the present claimed invention and the Examiner's allegations, element 9 of Mandai et al. is NOT a microstrip line, and certainly does **NOT** "define a microstrip line resonator" as recited in the present claimed invention. Furthermore, the only resonator disclosed in Mandai et al. is defined by the conductive film 4 and the grounding electrode films 3 and 5 disposed on both sides of the conductive film 4 (see col. 3, lines 38-44). Thus, Mandai et al. clearly fails to teach or suggest "a single resonator is defined by said microstrip line resonator and said strip line resonator" as recited in the present claimed invention.

Accordingly, Applicant respectfully submits that Mandai et al. fails to teach or suggest the unique combination and arrangement of elements recited in claims 1, 8 and 14 of the present application.

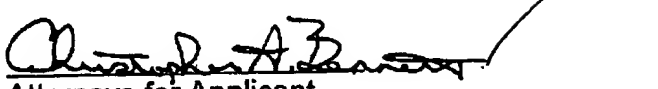
In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1, 8 and 14 are allowable. Claims 2-7, 9-13 and 15-21 depend upon claims 1, 8 and 14, and are therefore allowable for at least the reasons that claims 1, 8 and 14 are allowable.

In view of the foregoing Remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

To the extent necessary, Applicant petitions the Commissioner for a Two-month extension of time, extending to December 9, 2002, th period for response to the Office Action dated July 9, 2002.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,



Attorneys for Applicant

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

December 4, 2002

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080

VERSION WITH MARKINGS SHOWING CHANGES MADE

1. A resonator comprising:

a multi-layer substrate having an upper and lower surface, and including at least two conductor layers which include at least two grounding conductor layers and a plurality of dielectric layers, one of the at least two grounding conductor layers being disposed on the lower surface of the multi-layer substrate;

a strip line disposed between the at least two grounding conductor layers;

a microstrip line disposed on the upper surface of said multi-layer substrate; and

a through hole formed in said dielectric layers to connect said strip line to said microstrip line;

wherein at least a portion of the one of the at least two conductor layers that is closest to said microstrip line and faces the microstrip line is omitted;

said microstrip line defines a microstrip line resonator;

at least one of said plurality of dielectric layers, at least one of said at least two grounding conductor layers and said strip line define a strip line resonator; and

a single resonator is defined by said microstrip line resonator and said strip line resonator.

2. A resonator according to Claim 1, wherein said portion of said one of the at least two conductor layers that is omitted is disposed [inside] within said multi-layer substrate and is arranged such that said grounding conductor layer disposed on the lower surface of said multilayer substrate faces said microstrip line.

8. A resonator comprising:

a multi-layer substrate having an upper and lower surface, and including at least two conductor layers which include at least two grounding conductor layers and a plurality of dielectric layers, one of the at least two grounding conductor layers being disposed on the lower surface of the multi-layer substrat , and one of the at least two conductor layers that is closest to said microstrip line and faces th microstrip line has an opening formed th rein;

a strip line disposed between the at least two grounding conductor layers;

a microstrip line disposed on the upper surface of said multi-layer substrate; and

a through hole formed in said dielectric layers to connect said strip line to said microstrip line;

said microstrip line defines a microstrip line resonator;

at least one of said plurality of dielectric layers, at least one of said at least two grounding conductor layers and said strip line define a strip line resonator; and

a single resonator is defined by said microstrip line resonator and said strip line resonator.

14. A voltage controlled oscillator comprising:

a resonator including:

a multi-layer substrate having an upper and lower surface, and including at least two conductor layers which include at least two grounding conductor layers and a plurality of dielectric layers, one of the at least two grounding conductor layers being disposed on the lower surface of the multi-layer substrate;

a strip line disposed between the at least two grounding conductor layers;

a microstrip line disposed on the upper surface of said multi-layer substrate; and

a through hole formed in said dielectric layers to connect said strip line to said microstrip line;

wherein at least a portion of the one of the at least two conductor layers that is closest to said microstrip line and faces the microstrip line is omitted;

said microstrip line defines a microstrip line resonator;

at least one of said plurality of dielectric layers, at least one of said at least two grounding conductor layers and said strip line define a strip line resonator; and

a single resonator is defined by said microstrip line resonator and said strip line resonator; and

a plurality of electronic component elements disposed on the upper surface of the multi-layer substrate and arranged to define a circuit.

16. The voltage controlled oscillator according to claim 14, wherein said portion of said one of the at least two conductor layers that is omitted is disposed [inside] within said multi-layer substrate and is arranged such that said grounding conductor layer disposed on the lower surface of said multi-layer substrate faces said microstrip line.